NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Production

Revision 1.1: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52250STDR	Tape & Reel	4000	2250	8	SOP-8L

Over ope

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V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

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V_{IN}=12V, T_A= 25°C.

Figure 1. UVLO vs Temperature

Figure 2. Supply current vs Temperature

Figure 3.

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Overview

The SCT52250 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 5A peak current along with the minimum propagation delay 12ns from input to output. The 1ns delay matching and the stackable output characteristics

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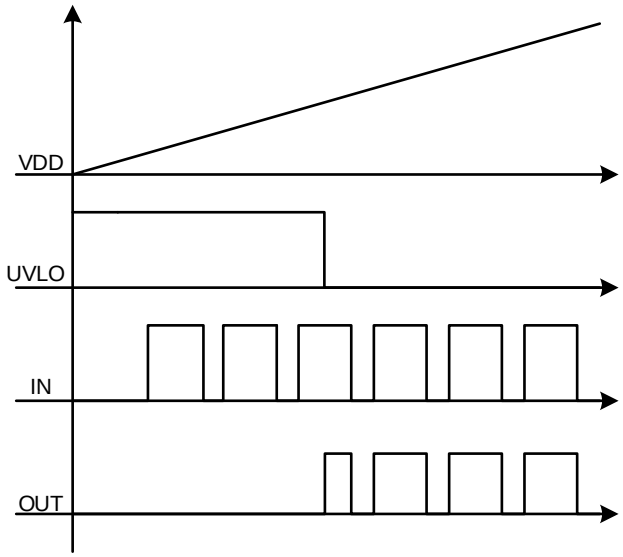

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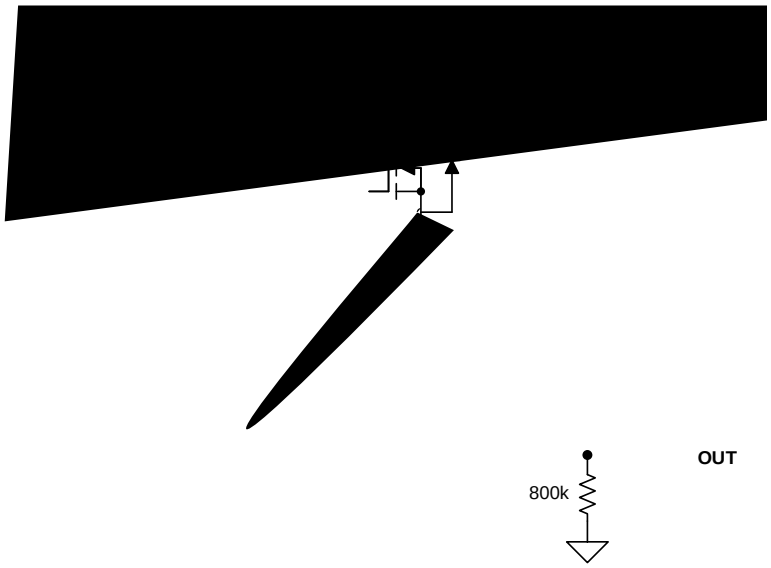

Figure 12

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Figure 13. SCT52250 Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

Figure 14. Driver Switching ON

Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52250 exceeds 162

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Typical Application

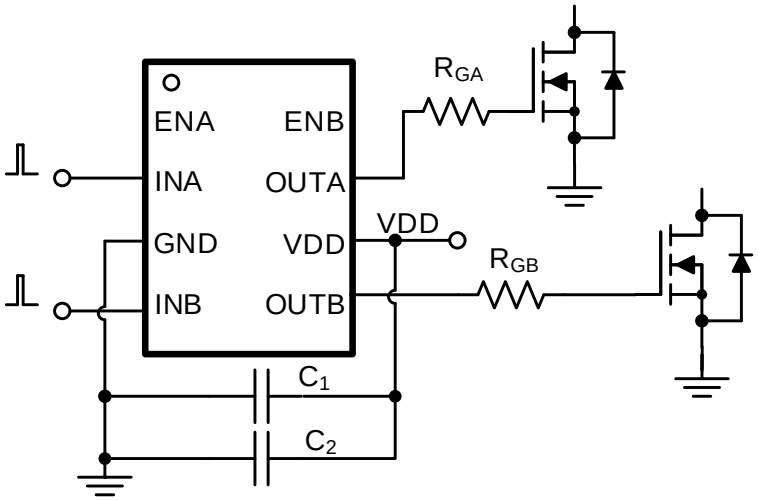

Figure 16. Dual Channel Driver Typical Application

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Driver Power Dissipation

Generally, the power dissipated in the SCT52250 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52250 features very low quiescent /Spbtrents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52250 is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52250 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT52250
- R_{OL} is the pull down resistance of SCT52250
- R_G is the gate resistance between driver output and gate of power device.

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/Spanoot-MCID 16/Lang (en-US) 6 9.96 Tf 311.45af03.83
/Spanoot-MCID 44/Lang (en-US) 6 9.96 Tf 311.45af19 54

Application Waveforms

VDD=12V unless otherwise noted

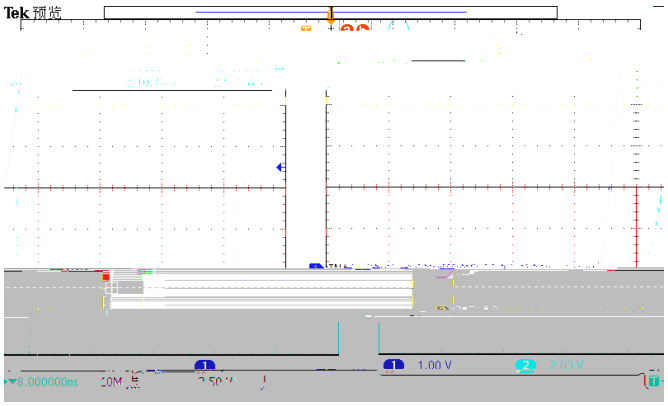

Figure 23. Stackable Output Rise (Out capacitance=3.3nF)

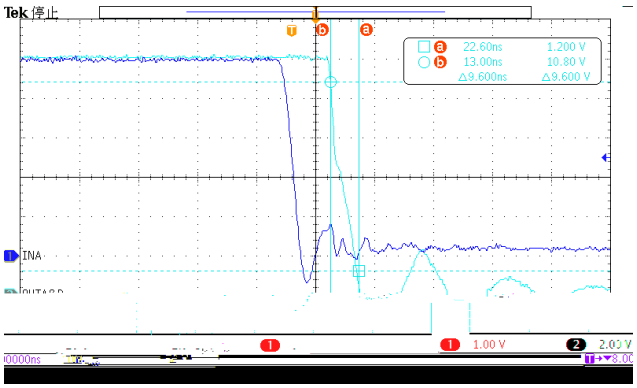

Figure 24. Stackable Output Fail (Out capacitance=3.3nF)

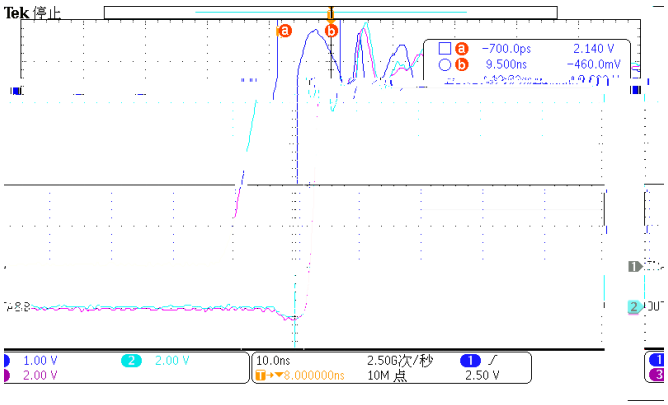

Figure 25. Delay Matching Rise (Out capacitance=1.8nF)

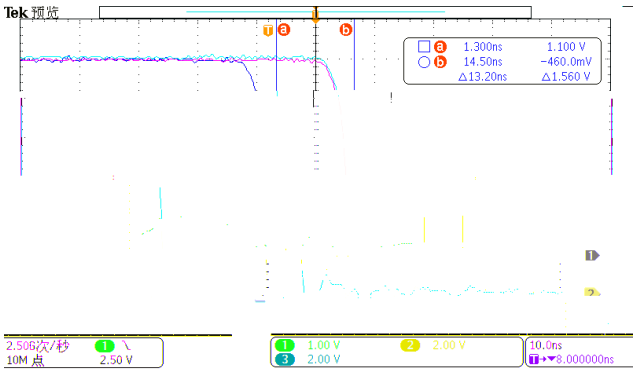

Figure 26. Delay Matching Fail (Out capacitance=1.8nF)

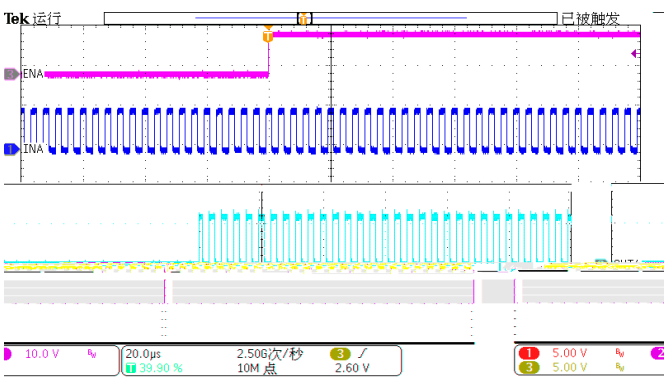

Figure 27. Enable

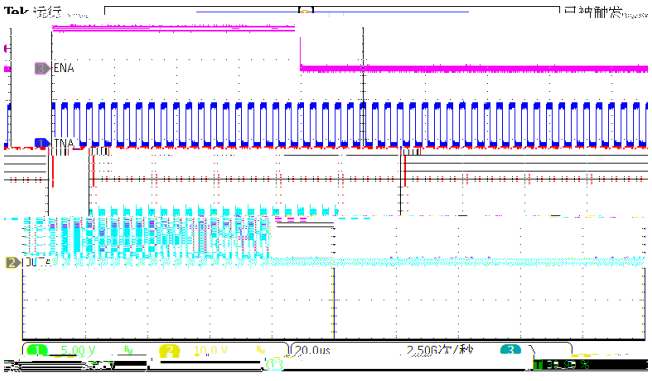

Figure 28. Disable

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Layout Guideline

The SCT52250 provides the 5A output driving current and features very short rdt12 0 612 3 and fall 3 ti12 0me at the power devices gate. The high di/dt causes driver output unexpectedin ng when the driver output loop dt12 0 not designed wel12 0l. The re3ulator couldt12 0uffer from malfunction and EMI dt12 0e dprobdf ds the power device dgate dhas t12 0erdous rd 3 6-6(3)]TJETQ EMC /Span <</MCID 11/Lang (en-US)>BDC q0.00000912 6-6(gu)4(n)-3(e)-8(23)4(2)6(9)]TJETQ EMC /Span <</MCID 24/Lang (en-US)>BDC q0.00000912

Put the SCT52250 as clas post12 0 612ble to the power device to minimize the gate driving lp 6-6(c)-3(l) 0uding the driver output and power devdce gate The power pl decoupl 6-6(3)]TJETQ EMC /Span <</MCID 23/Lang (en-US)>BDC q0.00000912

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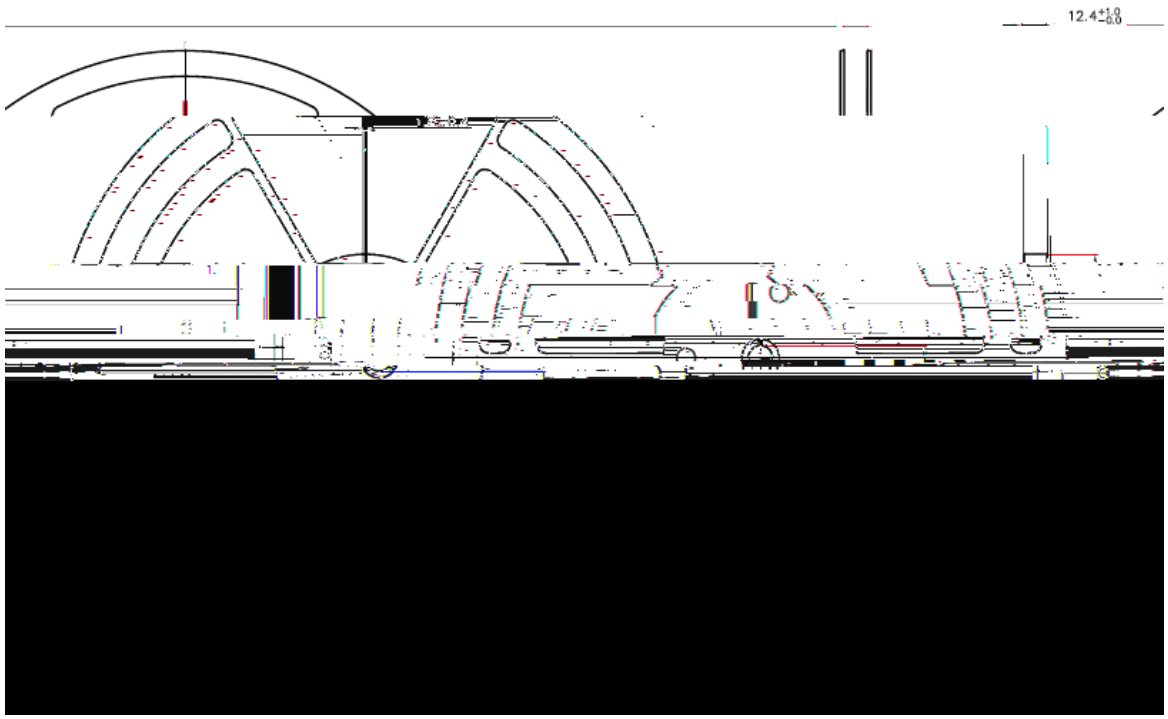

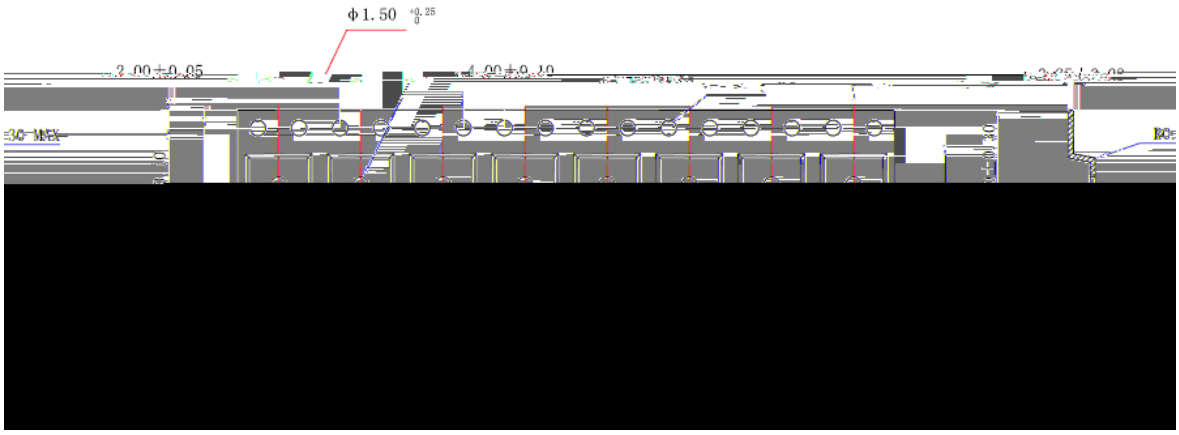

Feeding Direction

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